

REMARKS

Claims 1-3 and 5-40 were pending in the application.  
Please cancel claim 40, without prejudice or disclaimer.

The abstract is objected to as including the acronym DAG without any definition. The title of the application is objected to as being non-descriptive. The drawings are objected to as including a reference sign not mentioned in the description. Claims 8-14, 22, 33, 36, and 39 stand rejected as allegedly failing to comply with 35 U.S.C. 112.

Claims 1-3, 5-10, 16-18, and 20-40 stand rejected as allegedly being anticipated by Nair et al. "Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups," ("Nair"). Claims 11-14 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Nair in view of U.S. Patent No. 6,092,187 to Killian ("Killian"). Claim 15 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Nair in view of Ferreira de Souza "Dynamically Scheduling the Trace Produced During Program Execution into VLIW Instructions" ("de Souza").

In view of the amendments and remarks herein, the rejections are respectfully traversed. Reconsideration and allowance are respectfully requested.

I. The Objections to the Specification

The abstract of the disclosure has been amended as required in the office action. The title has been amended to be descriptive of the pending claims. In view of these amendments, the objections to the specification are rendered moot.

## II. The Objection to the Drawings

The specification has been amended to reference element 414 found in the figures. In view of these amendments, the objects to the drawings are rendered moot.

## III. The Rejections under 35 U.S.C. 112

The claims have been amended to provide proper antecedent basis. Therefore, the rejections under 35 U.S.C. 112 are rendered moot.

## IV. The Rejections under 35 U.S.C. 102 and 103

Independent claims 1, 20, and 29 have been amended to more clearly emphasize a combination of patentable features of the current disclosure.

### Claim 1

For example, independent claim 1 includes the feature that "each of the plurality of traces including information indicative of interdependent instructions." The cited references, particularly Nair, neither teach nor suggest this feature of claim 1.

Nair is directed to a dynamic scheduling concept, where groups of instructions may be pre-formatted and cached for subsequent execution by a parallel engine. Turning to the example used in the office action, Figure 7 of Nair shows a number of groups that may be formed using the systems and techniques described in that reference. As Figure 7 illustrates, the groups of Nair do not all include criterion instructions, as recited in claim 1. For example, the group in slot 4 includes an addition operation and a store operation and does not include either a branch instruction or a load instruction.

In contrast, claim 1 recites a cache of trace information associated with a plurality of traces, where each of the plurality of traces includes at least a criterion instruction and an associated instruction, where the criterion instruction and the associated instruction are interdependent. A cache according to claim 1 may thus be used to speculatively execute the interdependent instructions to avoid, for example, misdirection at a branch, or a cache miss.

Further, there is no motivation in the references to modify Nair to include the features of claim 1, and in fact doing so changes the principle of operation of Nair. Therefore, such a modification is not obvious (please see MPEP 2143.01). The

dynamic scheduling concept of Nair allows for groups to be cached, where the groups are reformatted in a form convenient for direct execution by a parallel engine (please see page 14, column 1 of Nair). Once the groups are cached, they may be fetched for parallel execution if they are encountered again. (Please see page 14, column 1 of Nair). Thus, Nair is directed to the idea of pre-formatting sets of instructions and caching them for parallel execution, and does not require that the sets of instructions include a criterion instruction. Modifying Nair so that each trace includes a criterion instruction would change the character of the groups allowed in Nair, and thus affect the amount of parallelism that may be achieved. Thus, such a modification is not obvious.

Claims 2-19 and 32-34

Claims 2-19 and 32-34 depend from claim 1, and are therefore patentable for at least the reasons stated above with respect to claim 1.

Claims 20-31 and 35-39

Claim 20 has been amended to recite both "identifying a pre-selected number of initial candidate instructions preceding the criterion instruction in the program sequence," and "determining which of the initial candidate instructions ~~and the~~ are associated instructions, wherein an outcome of the criterion

instruction depends on the results of the associated instructions."

An exemplary implementation including these features is discussed on page 9 of the specification. In that example:

"DAG extractor 30 then captures these criterion instructions and their respective associated instructions by sliding an analysis window of a predetermined size down the original instruction sequence. When an identified criterion instruction moves into the bottom of the window, all the instructions in the window are captured as initial candidate instructions for a DAG trace, since potentially, the criterion instruction is data dependent upon all of them. Trace builder 21 examines the captured instructions and discards those having no interdependency relationship with the criterion instruction."

The references neither teach nor suggest these features of claim 20. As noted above, Nair is directed to a dynamic scheduling concept, where groups of instructions may be pre-formatted and cached for subsequent execution by a parallel engine. Figure 7 of Nair illustrates that the groups need not include criterion instructions. For the groups that do include criterion instructions, Nair neither teaches nor suggests identifying a pre-selected number of initial candidate instructions preceding the criterion instruction in the program sequence.

As also noted above, it is not obvious to modify Nair to include the above features of claim 20, since doing so would change the principle of operation of Nair.

Claims 21-28 and 35-37

Claims 21-28 and 35-37 depend from claim 20, and are therefore patentable for at least the same reasons as stated above with respect to claim 20.

Claim 29 includes features similar to those discussed above with respect to claim 20, and is therefore patentable for similar reasons. Claims 30, 31, 38, and 39 depend from claim 29, and are therefore patentable for at least the same reasons as stated above with respect to claim 29.

CONCLUSION

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue, or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any

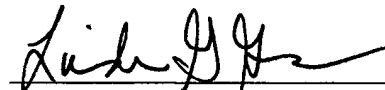
claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the above amendments and remarks, therefore, all of the claim should be in condition for allowance. A formal notice to that effect is respectfully solicited. If the Examiner has any questions regarding this response, the Examiner is invited to telephone the undersigned at (858) 678-5070.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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